REMARKS/ARGUMENTS

Applicants acknowledge receipt of the Office Action dated September 5, 2003 in the parent case. In that Action, the Examiner: 1) rejected claim 1 as allegedly unpatentable over *Joseph* (U.S. Pat. No. 6,338,123); 2) rejected claims 2-4, 10-12, 14, 16 and 19 as allegedly unpatentable over *Joseph* in view of *Baylor* (U.S. Pat. No. 5,778,437); 3) rejected claim 20 as allegedly unpatentable over *Joseph* in view of *Cai* (U.S. Patent No. 5,953,512); and 4) objected to claims 13, 15, 17, 18, 21 and 22 for being dependent upon a rejected base claim, but otherwise allowable.

With this Preliminary Amendment, Applicants cancel claims 5-9, as those same claims were cancelled in the parent case. Further, Applicants amend claims 1-3 to make those claims read the same as the corresponding claims in the parent case for the last Office action. Applicants further amend claim 1 as discussed below. Finally, Applicants add new claims 10-16, which correspond directly to claims 10-12, 14, 16, 19 and 20 in the parent case. Applicants believe the pending claims are allowable over the art of record and respectfully request reconsideration.

I. AMENDMENTS TO THE SPECIFICATION

With this Preliminary Amendment, Applicants amend the specification to note the Serial Numbers, and in some cases corrected titles, of the related applications. Further, Applicants note the continuation status of the current application. No new matter is submitted by these amendments.

II. CLAIMS REJECTIONS

A. Claim 1

Claim 1 is directed to a distributed multiprocessing computer system that comprises, *inter alia*, an I/O bridge that obtains exclusive ownership of shared memory module data blocks during I/O device accesses. The Examiner rejected claim 1 as allegedly obvious over *Joseph*. Applicants amend claim 1 to more clearly define that the I/O bridge is an active participant in the directory-based coherence protocol by requiring that the I/O bridge obtains exclusive ownership of shared memory module data blocks during I/O device accesses.

In rejecting claim 1, the Examiner cites *Joseph's* Background section. The paragraph cited by the Examiner, as well as the preceding paragraph, is reproduced below (with that portion of the paragraph emphasized by the Examiner in bold):

> Conventional computer systems often include on-chip or off-chip cache memories which are used with processors to speed up accesses to system memory. In a shared memory multiprocessor system, more than one processor can store a copy of the same memory location(s) (or line(s)) in its cache memory. A cache coherence mechanism is required to maintain consistency among the multiple cached copies of the same memory line. Furthermore, a network protocol such as a Sealable Coherent Interface (SCI) is often used in conjunction with the conventional systems.
>
> In small, bus-based multiprocessor systems, the coherence mechanism is usually implemented as part of the cache controllers using a snoopy coherence protocol. The snoopy protocol cannot be used in large systems that are connected through an interconnection network due to the lack of a bus. As a result, these systems use **a directory-based protocol to maintain cache coherence.** The directories are associated with the main memory and maintain the state of information of the various caches on the memory lines. This state information includes data indicating which cache(s) has a copy of the line or whether the line has been modified in the caches.

Joseph, Col. 1, lines 14-35 (emphasis added). Thus, the location cited by the Examiner does not teach or fairly suggest that the I/O bridge, as opposed to the processors, should obtain exclusive ownership of shared memory module data blocks during I/O device access.

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-4), should be allowed.

B. Claim 2

Claim 2 is directed to a distributed multiprocessing computer system having all the limitations of claim 1 and further requiring that data blocks transferred during an I/O write access may be buffered by the I/O bridge only if the I/O bridge has exclusive copies of the data blocks. The Examiner rejected claim 2 as allegedly obvious *Joseph* in view of Baylor.

The teachings of *Baylor* at the locations cited, Col. 8, lines 5-25 (which are in *Baylor's* claims), do not seem to logically follow the limitations at issue.

Applicant's claim 2 requires that "data blocks transferred during an I/O device write access may be buffered by the I/O bridge only if the I/O bridge has exclusive copies of the data blocks." The cited claim section of *Baylor* does not mention an I/O bridge, or that buffering should take place by the I/O bridge only if it has exclusive copies.

Based on the foregoing, Applicants respectfully submit that the combination of *Joseph* and *Baylor* does teach or fairly suggest the limitations of claim 2.

C. Claim 10

Claim 10 is directed to a method that comprises, *inter alia,* maintaining coherency between the memories of multiple processors and a cache of an I/O bridge device that caches data blocks from at least one of the memories. The Examiner rejected claim 10 as allegedly obvious over *Joseph* in view of *Baylor.* However, the rejection for claim 10 reads, in its entirety, as follows:

> Claims 10, 14, 16 and 19 have similar limitations as claim 1. Joseph et al. teach apparatus as set forth in claim 1. Therefore, Joseph et al. also teach method and apparatus as set forth in claims 10 and 14, 16 and 19 respectively.

Office Action Dated September 5, 2003, page 4, paragraph 8.

Thus, while the Examiner in one paragraph indicates that the rejection of claim 10 is an obviousness rejection based on *Joseph* and *Baylor*, the specifics of the rejection seem to imply that claim 10 is rejected for the same reasons as claim 1, over *Joseph* alone.

Further, the only cite to the *Baylor* reference (in the rejection of claim 2) is *Baylor's* Col. 8, lines 5-25, the claims of *Baylor.* However, the location cited in *Baylor* discusses only "a processor attempting to modify data." *Baylor*, Col. 8, lines 6-7. There is no discussion that an I/O bridge may have a cache memory or that the I/O bridge itself could cache data blocks. Thus, the combination of *Joseph* and *Baylor* does not teach or fairly suggest the limitations of claim 10.

Based on the foregoing, Applicants respectfully submit that claim 10 and all claims which depend from claim 10 (claims 11-12), should be allowed.

D. Claims 13 and 14

Claim 13 requires, *inter alia*, an I/O bridge device coupled to a plurality of processors, and wherein the I/O bridge device sends interrupt requests to a target processor using message packets. The target processor of claim 13 reads the message packets to determine the source of the interrupt. Claim 14 requires, *inter alia*, a computer system having an I/O bridge that is adapted to perform speculative prefetching of data blocks from the memory modules during direct memory access writes from an I/O device. The Examiner rejected claims 14 and 16 in the parent case (now claims 13 and 14) as allegedly obvious over *Joseph* in view of *Baylor*. However, the rejection reads, in its entirety, as follows:

> Claims 10, 14, 16 and 19 have similar limitations as claim 1. Joseph et al. teach apparatus as set forth in claim 1. Therefore, Joseph et al. also teach method and apparatus as set forth in claims 10 and 14, 16 and 19 respectively.

Office Action Dated September 5, 2003, page 4, paragraph 8.

Claim 13 requires an I/O bridge device adapted to send interrupt requests to a target processor. Claim 14 requires an I/O bridge device configured to perform prefetching of data blocks. These limitations are not found in claim 1, and thus reliance in the Office Action on the rejections with respect to claim 1 is misplaced.

Based on the foregoing, Applicants respectfully submit that the Office Action dated September 5, 2003 fails to make a *prima facia* case of obviousness with respect to claims 13 and 14, and these claims should therefore be allowed.

E. Claim 15

Claim 15 is directed to a bridge logic device that comprises, *inter alia,* a direct memory access (DMA) hardware logic that comprises a cache buffer that stores memory blocks during DMA reads and writes. The Examiner rejected claim 15 in the parent case (claim 15 herein) as allegedly obvious over *Joseph* in view of *Baylor*. However, the rejection refers only to the rejections with respect to claim 1, a Section 103 rejection over *Joseph* alone.

Notwithstanding the inconsistencies in the rejections, Applicants respectfully submit that neither *Joseph* standing alone, nor *Joseph* in combination with *Baylor,* teach or fairly suggest all the limitations of claim 15. In particular, neither *Joseph* nor *Baylor*, alone or in combination, teach or fairly suggest that a bridge logic device should have a DMA hardware logic comprising a cache buffer that participates in the directory based coherence protocol to maintain coherency of memory blocks stored in the cache buffer.

Based on the foregoing, Applicants respectfully submit that claim 15, as well as claim 16 which depends from claim 15, should be allowed.

III. CONCLUSION

Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Mark E. Scott
PTO Reg. No. 43,100
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400